REMARKS

Claims 1-24 remain pending. In the present Office Action, claims 1-8 and 11-24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Pontius et al., U.S. Patent No. 6,029,243 ("Pontius"). Claims 9-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pontius in view of allegedly well known features, using a publication attached to the Advisory Action of June 26, 2006 as evidence. Applicants respectfully traverse these rejections and request reconsideration

Applicants respectfully submit that each of claims 1-24 recite combinations of features not taught or suggested in the cited art. Furthermore, Applicants submit that the remarks made in the Response to Final Action filed May 25, 2006 (and apparently received in the USPTO on May 30, 2006) illustrate reasons why claims 1-24 are not taught in the cited art. Applicants **incorporate those remarks by reference to preserve them for appeal**. Applicants provide additional remarks below, and also respond to certain assertions from the Advisory Action mailed June 26, 2006 (the "Advisory Action", herein).

Claim 1 recites a combination of features including: "a scheduler configured to schedule the floating point operation for execution, wherein the prediction circuit is configured to predict the execution latency prior to the floating point operation being scheduled by the scheduler for execution." The present Office Action alleges that Pontius teaches the above features, asserting that the prediction must be made prior to the scheduling for the processor to determine if the instruction is to be scheduled to the execution unit or the software trap (See Office Action, page 3, fourth full paragraph). Applicants respectfully disagree. A trap is normally signalled in a processor during execution of the instruction. There is no need to know, prior to scheduling the instruction for execution, whether or not the instruction will trap.

Additionally, the Office Action asserts that the scheduler recited in claim 1 is the control device that uses the LAD and LAE information to determine the mechanism for executing the floating point instruction (See Office Action, page 3, second full

paragraph). However, the trap logic TPL detects the trap based on the operands read from the register bank. The operands read from the register bank are also provided directly to the execution unit EXU for execution (see Fig. 1, INA and INB). Thus, it is very clear that the operation of the TPL unit to detect the trap in the LAE occurs after the instruction is scheduled for execution. This contradicts the assertion in the Office Action, since the scheduler must schedule the instruction for execution without the LAE/LAD information. Still further, the Office Action asserts that the TPL is part of the floating point execution unit (see Office Action, page 3, fifth full paragraph). Again, this contradicts the above assertion.

Still further, the Office Action asserts that Pontius inherently predicts the execution latency based on the requested result precision (See Office Action, page 2, last paragraph extending to page 3). Applicants respectfully disagree. The requested result precision, along with certain operand bits, are used by the LAE and LAD in the TPL to detect a hardware-unsupported precision to signal a trap. No prediction is made…rather the op is decoded and the requested precision is provided at execution time. For example, Pontius teaches: "Logic for selecting execution precision is used to determine whether an operation is to be performed in hardware or in software (in response to a trap). A simple approach is to set the execution precision equal to the maximum of the requested result precision and the maximum apparent precision of the operands. When the execution precision is within the capability of the execution unit, the operation is performed in hardware; when the execution precision is too high for the execution unit, a trap is executed to initiate execution in software. In this approach, a high requested result precision always results in a trap." (Pontius, col. 2, line 60-col. 3, line 3). This discussion is part of the summary, and is effectively discussing the operation of the LAE and LAD in the TPL. Clearly, the above discussion refers to using the requested precision at execution time to determine if a trap is signalled or not. There is no teaching or suggestion that the requested precision is used at any other time to make any sort of prediction.

For at least all of the above stated reasons, Applicants respectfully submit that claim 1 is patentable over the cited art. Claims 2-15, dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 2-15 recite additional combinations of features not taught or suggested in the cited art. **Applicants reserve the right to highlight such additional features on appeal.**

Claim 16 recites a combination of features including: "scheduling the floating point operation from a scheduler for execution in a floating point unit wherein the predicting is performed prior to the scheduling". The same teachings of Pontius highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 16. Applicants respectfully submit that Pontius does not teach or suggest the combination of features recited in claim 16, either. Accordingly, claim 16 is patentable over the cited art. Claims 17-24, being dependent from claim 16, are patentable over the cited art for at least the above stated reasons. Each of claims 2-15 recite additional combinations of features not taught or suggested in the cited art. **Applicants reserve the right to highlight such additional features on appeal.**

As noted in the Response to Final Office Action with regard to claim 8, merely measuring the latency from any desired point in the pipeline does not teach or suggest the "the prediction circuit is configured to PREDICT the execution latency of the floating point operation responsive to dispatch of the floating point operation to the scheduler". The Advisory Action asserts that the LAE and LAD hardware is used to make the prediction, and the information is utilized to schedule the instruction. However, as pointed about above, the LAE and LAD hardware operate at execution time to determine the precision. The assertion that the LAE and LAD hardware are considered to be a scheduler, as alleged in the Advisory Action, conflicts with the Office Action's assertion that the TPL (which includes the LAE and LAD hardware) is part of the floating point execution unit.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-91300/LJM.

Respectfully submitted,

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